REMARKS

Applicants respectfully request reconsideration of this application as amended. Claims 1-7, 10-16, and 19-25 have been amended. Claims 8, 9, 17, 18, 26, and 27 have been cancelled without prejudice. Claims 28-30 have been added. Therefore, claims 1-7, 10-16, 19-25, and 28-30 now are presented for examination.

Drawing Objections

Figures 1-9 have been objected to as being considered prior art. Figures 1-5 have been amended to indicate that they are prior art.

However, Figures 6-9 have not been amended. Figures 6-9 disclose, as recited in claim 1, responding to an occurrence of a fault in the first processor, transferring control of the first bus to the second processor via hardware associated with the first processor and the second processor. Using hardware to transfer control between processors is one embodiment of the present invention, therefore Figures 6-9 cannot be considered prior art.

Applicants respectfully request that the objections to Figures 1-9 be withdrawn. Applicants also welcome any explanation from the Examiner with regard to the objections to Figures 1-9.

Figure 7 has been objected to for failing to include the reference signs "701" and "710" mentioned in the description, and reference character "715" has been used to designate both communication modules and a P2P bridge control module. Applicants submit that figure 7 has been amended to appear in proper condition for allowance.

Figure 8 has been objected to because the description of item "810" should be changed from "DEFAULT DETECTION" to "FAULT DETECTION", and because the

power and reset control module "830" was not included. Applicants submit that figure 8 has been amended to appear in proper condition for allowance.

Figure 10 has been objected to because the description of item "1020" should be changed from "PREFORM BACKUP MODE BOOT PRECESS" to "PREFORM ACTIVE MODE BOOT PROCESS." Applicants submit that figure 10 has been amended to appear in proper condition for allowance.

Claim Objections

Claim 4 stands objected to because of the following informalities: Claim 4 recites the limitation "neither split mode or cluster mode" line 7. With respect to claim 4, as recommended by the Examiner, Applicants proposes amendment to the claim to overcome the objection. Accordingly, Applicants respectfully requests that the objection to claim 4 be withdrawn.

35 U.S.C. § 112 Rejection

Claims 2-6, 11-15, and 19-27 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Claims 2, 3, 5, 11, 12, 19, 20, and 21 have been amended to more particularly point out and distinctly claim the subject matter Applicants regard as the invention. Accordingly, Applicants respectfully request the rejection of these claims be withdrawn.

Claims 3-6, 12-15, and 21-24 inherit the deficiencies of their respective base claims. With regard to claims 3-6, 12-15, and 21-24, they depend from claims 2, 11, and 20. Claims 2, 11, and 20 have been amended for allowance, therefore claims 3-6, 12-15, and 21-24 are also in condition for allowance. Accordingly, Applicants respectfully request the rejection of claims 3-6, 12-15, and 21-24 be withdrawn.

35 U.S.C. § 102 Rejection

Claims 1, 8, 10, and 17 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lanus, U.S. Patent No. 6,112,271 ("Lanus"). Claims 8 and 17 have been cancelled without prejudice.

Lanus discloses an "*active/active configuration*, the multiconfiguration backplane has a first system processor board inserted into the first system processor slot and a second system processor board inserted into the second system processor slot. Each of a first set of one or more input/output boards is inserted into one of the first set of one or more input/output slots, and each of a second set of one or more input/output boards is inserted into one of the second set of one or more input/output slots. A first bridge board is inserted into the first bridge slot, and a second bridge board is inserted into the second bridge slot." (col. 3, lines 8-17). Lanus further discloses "if there is a failure in the system processor on COMPACTPCI Bus[1], *the processing load is shifted to system processor[2] in a second shared mode.*" (col. 5, lines 29-31).

In contrast, claim 1 recites, detecting faults via hardware associated with the first processor and the second processor, wherein the hardware includes a Redundant Host Controller, and responsive to an occurrence of a fault in the first processor, transferring control of the first bus to the second processor via hardware associated with the first processor and the second processor, wherein the hardware includes a Redundant Host Controller. Lanus discloses transferring system control upon failure of a processor, however Lanus does not teach or reasonably suggest using hardware to detect or perform the transfer. Instead, Lanus discloses using an active/active configuration, which is preformed by software drivers. Accordingly, Applicants respectfully request, for at least

the reasons set forth above, the rejection of claim 1 and its dependant claims be withdrawn.

With regard to claim 10, it contains limitations similar to those of claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection of claim 10.

Claims 1-27 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hammersley, U.S. Patent No. 6,618,783 ("Hammersley"). Hammersley discloses "a method for a first processor that controls I/O traffic of a first PCI bus to acquire and relinquish control of a second PCI bus when a second processor for doing the same becomes inoperative." (col. 8, lines 13-17).

In contrast, claim 1 recites, detecting faults via hardware associated with the first processor and the second processor, wherein the hardware includes a Redundant Host Controller, and responsive to an occurrence of a fault in the first processor, transferring control of the first bus to the second processor via hardware associated with the first processor and the second processor, wherein the hardware includes a Redundant Host Controller. Hammersley does teach transferring control of inoperative processors, however Hammersley does not does specify what software or hardware the system uses nor how the software or hardware is used. Specifically, Hammersley does not teach or reasonably suggest using a Redundant Host Controller to transfer control. Accordingly, Applicants respectfully request, for at least the reasons set forth above, the rejection of claim 1 and its dependant claims be withdrawn.

With regard to claims 10 and 19, they contain limitations similar to those of claim 1. Accordingly, Applicants respectfully request the rejection of claims 10 and 19 and their dependant claims be withdrawn.

35 U.S.C. § 103 Rejection

Claims 9, 18, and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hammersley in view of CompactPCI, Redundant System Slot Specification ("RSS Specification").

Claims 9, 18, and 27 have been cancelled without prejudice.

Conclusion

Applicants submit that claims as amended are now in condition for allowance. Accordingly, Applicants respectfully request that the rejections be withdrawn and the application be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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